

KEY INPUT SECTION ROM RAM 5 DISPLAY SECTION (INCLUDING AN OPTICAL SYSTEM) DIGITAL CAMERA SECTION CPU 9 CARD I/F RGB CABLE CARD I/F DISPLAY DEVICE MEMORY DEVICE SPU INPUT RAM

Fig. 3

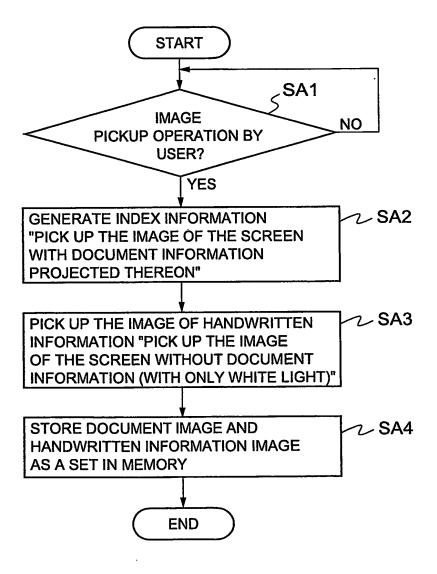


Fig. 4A

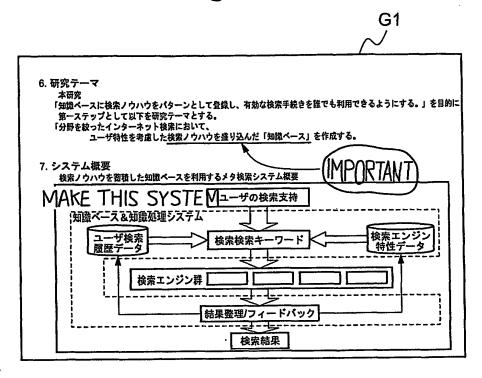
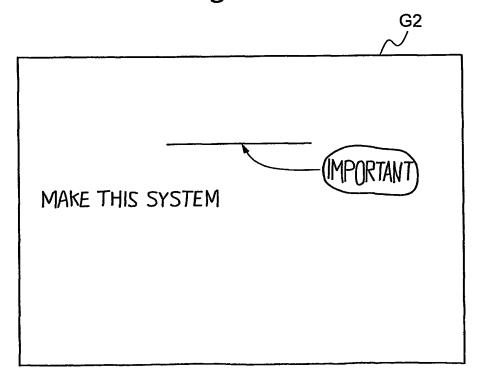
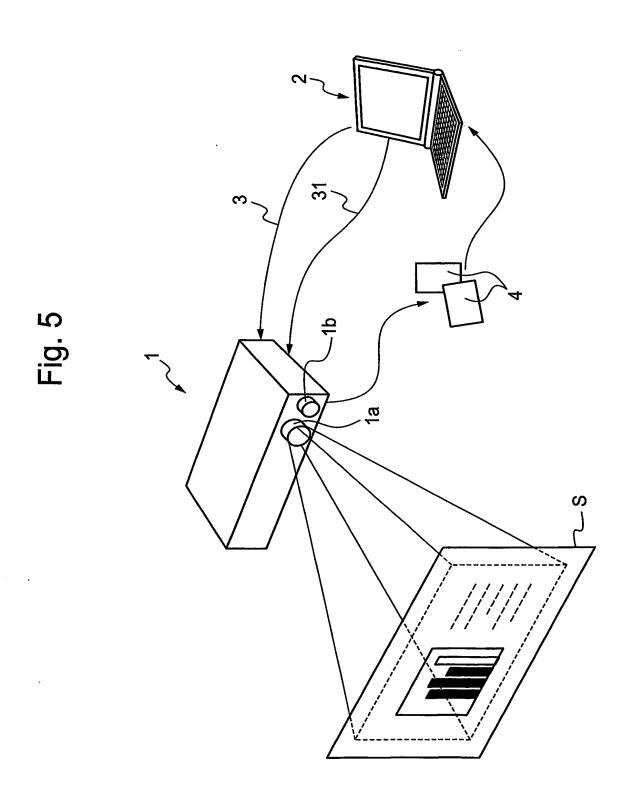


Fig. 4B





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KEY INPUT SECTION ROM RAM DISPLAY SECTION (INCLUDING AN OPTICAL SYSTEM) DIGITAL CAMERA SECTION SPU 16 CARD I/F Fig. 6 RGB CABLE CARD I/F ∑ 26 DISPLAY DEVICE MEMORY CPU INPUT DEVICE RAM

Fig. 7

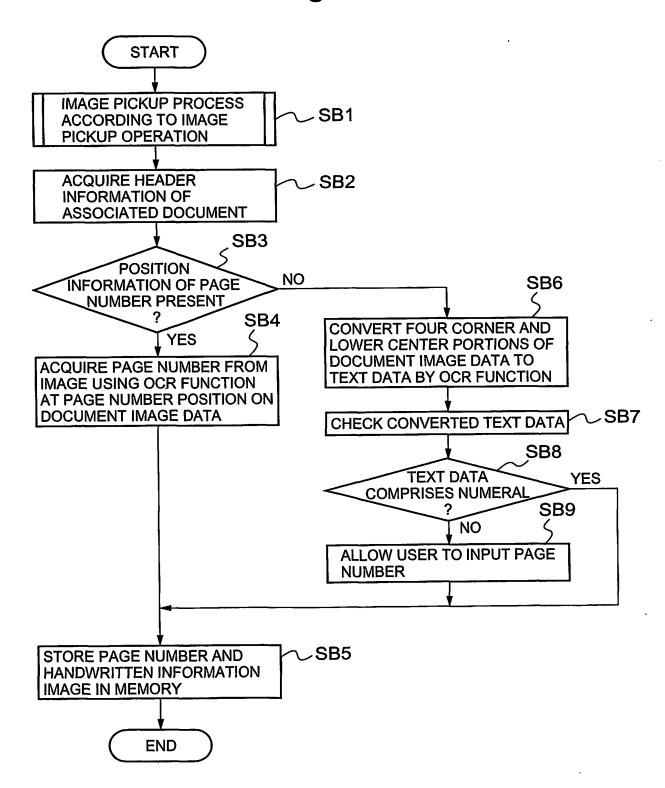


Fig. 8

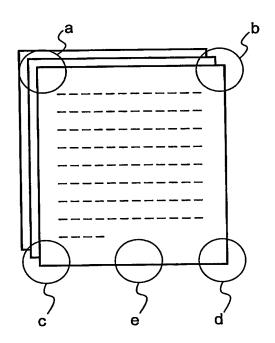


Fig. 9

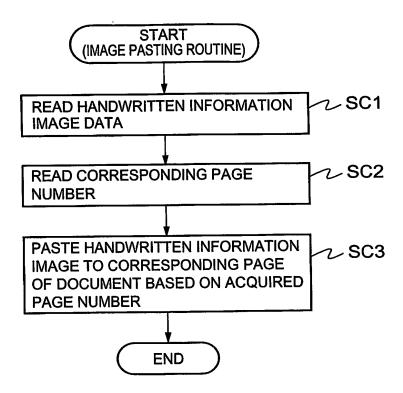


Fig. 10

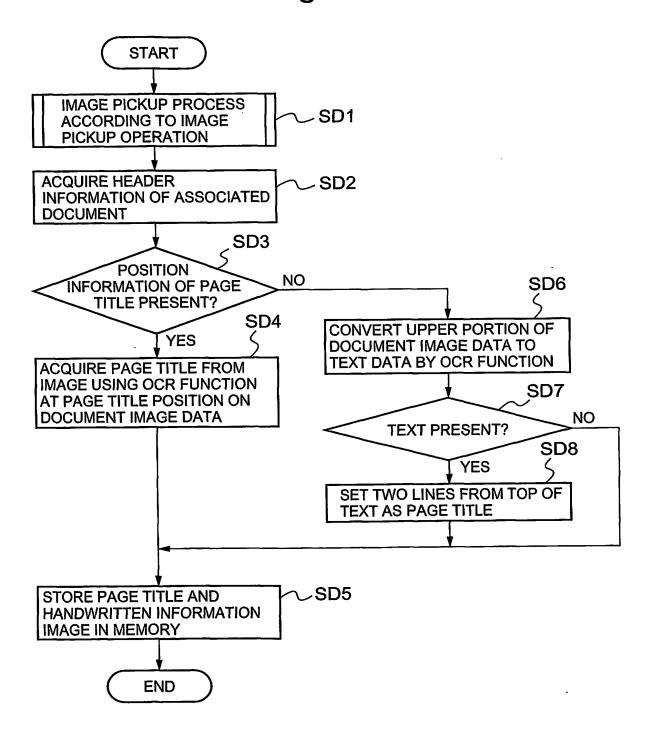


Fig. 11

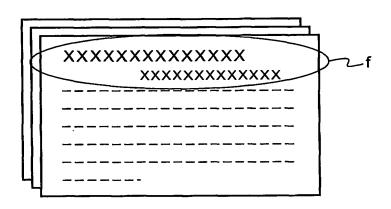


Fig. 12

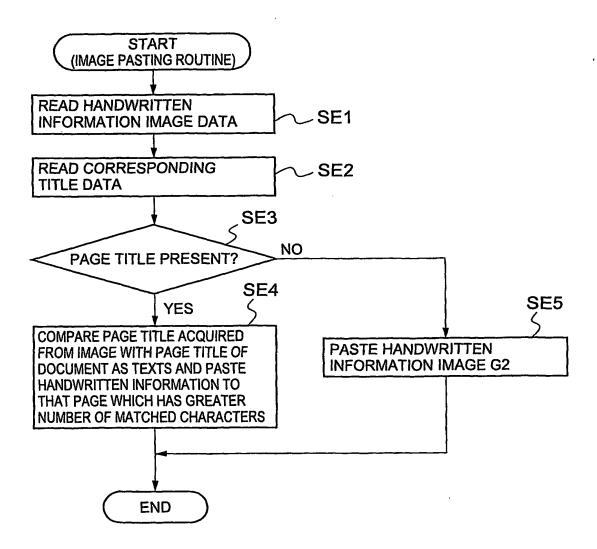


Fig. 13

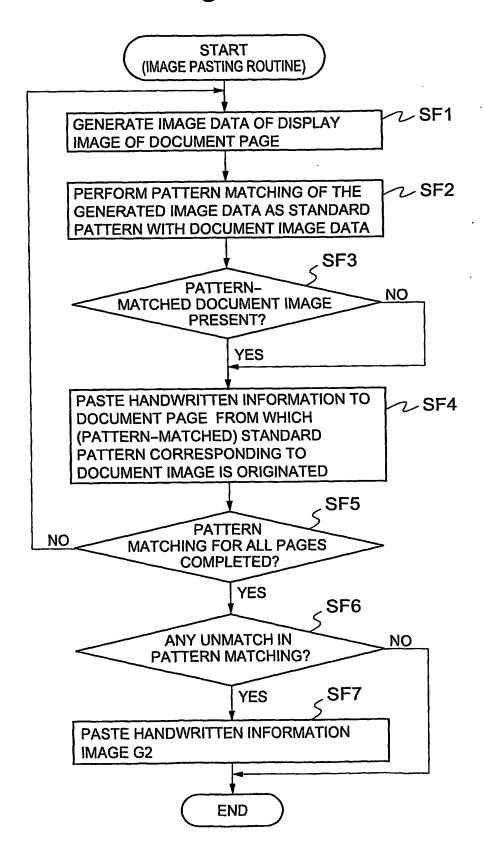
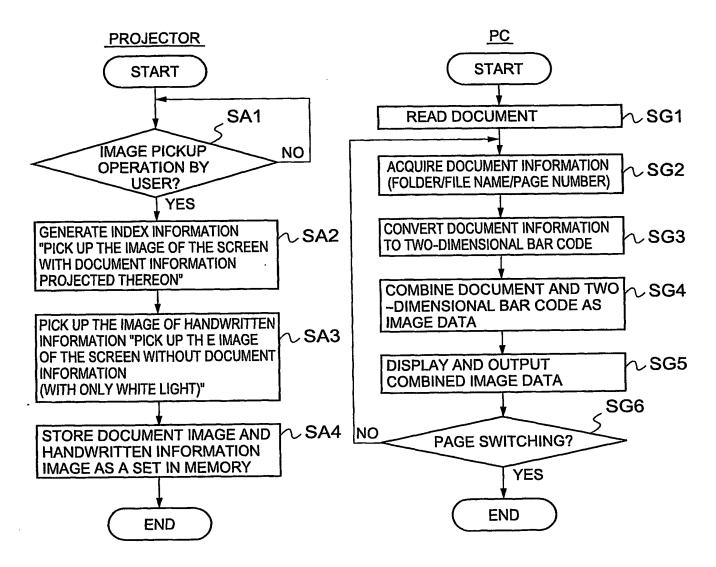


Fig. 14



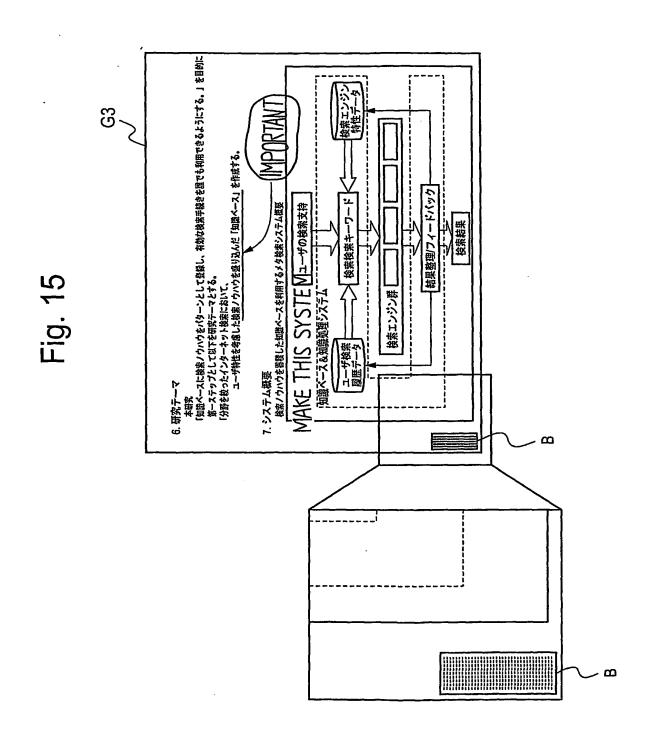


Fig. 16

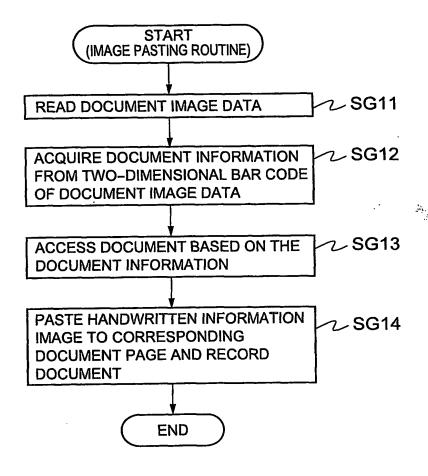


Fig. 17

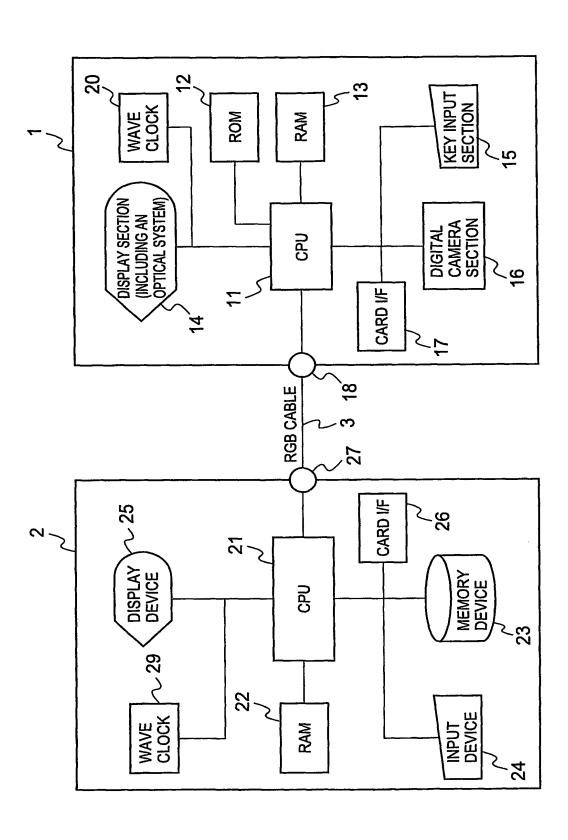
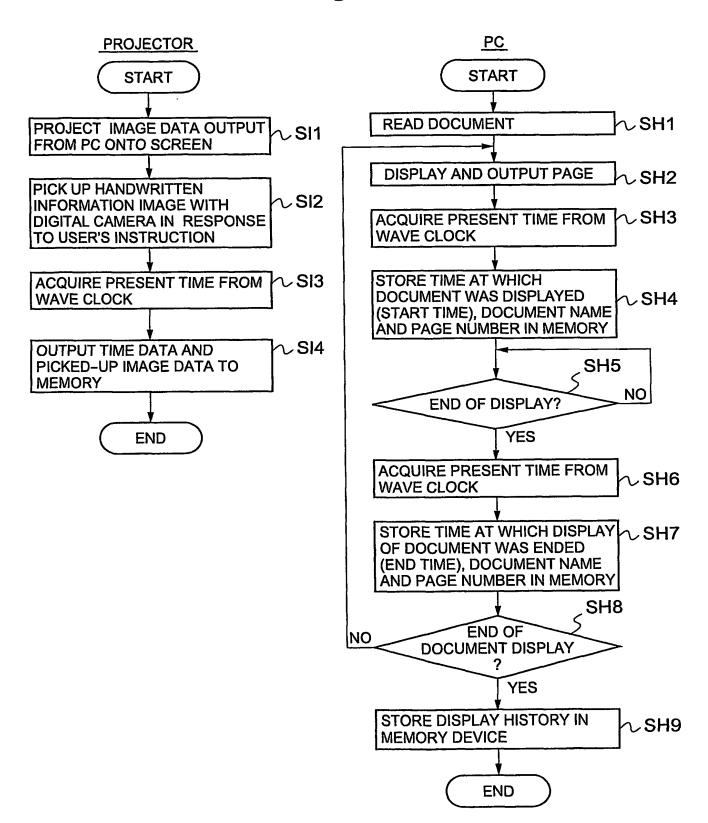


Fig. 18



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START/END FLAG

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START TIME

END TIME

Fig. 19

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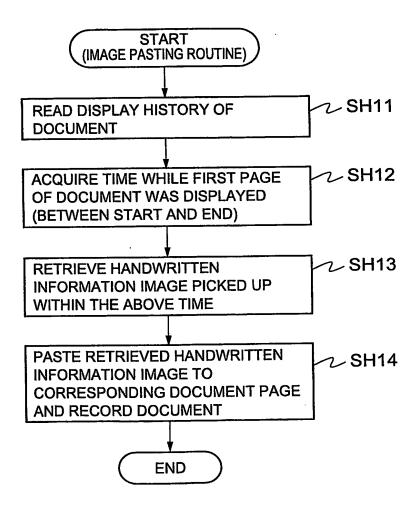
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Fig. 20



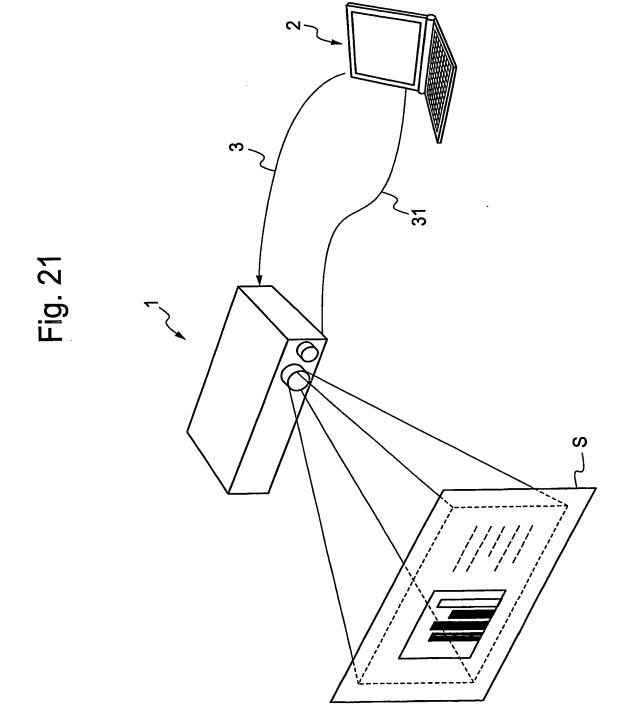


Fig. 22

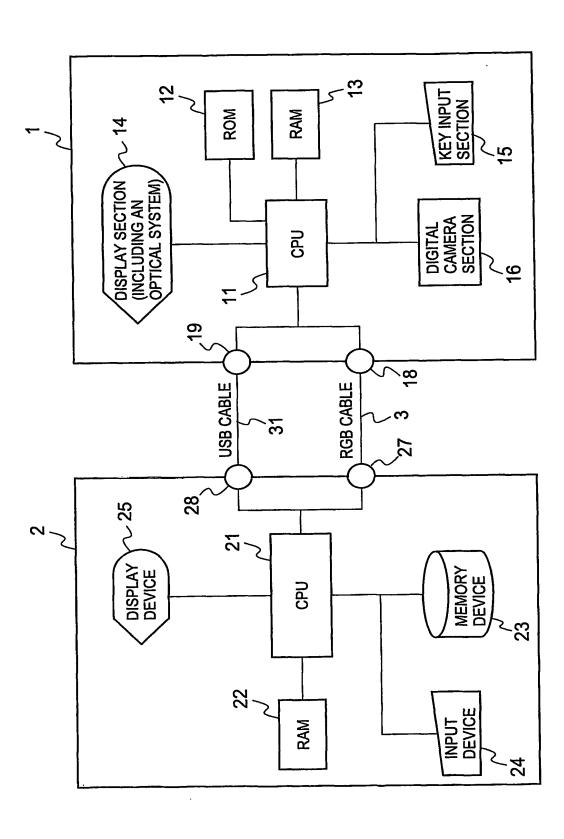


Fig. 23

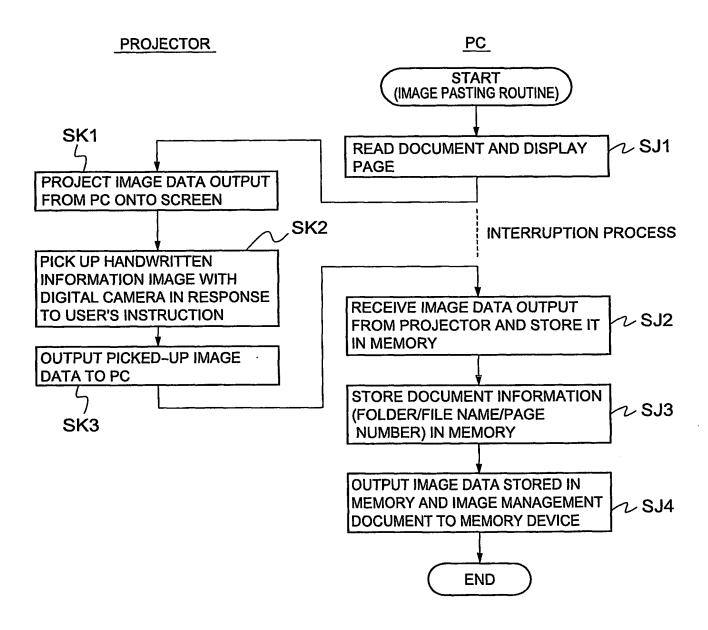


Fig. 24

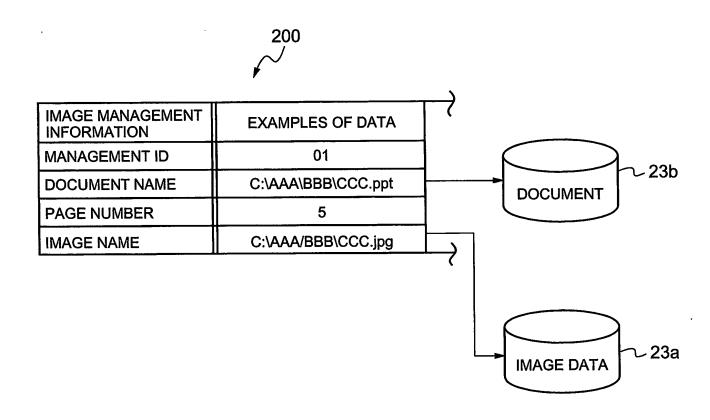


Fig. 25

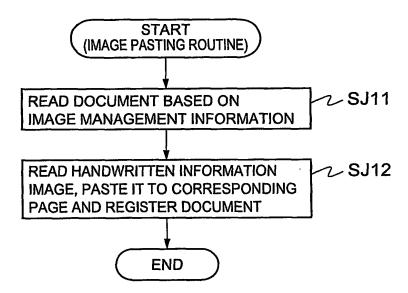


Fig. 26

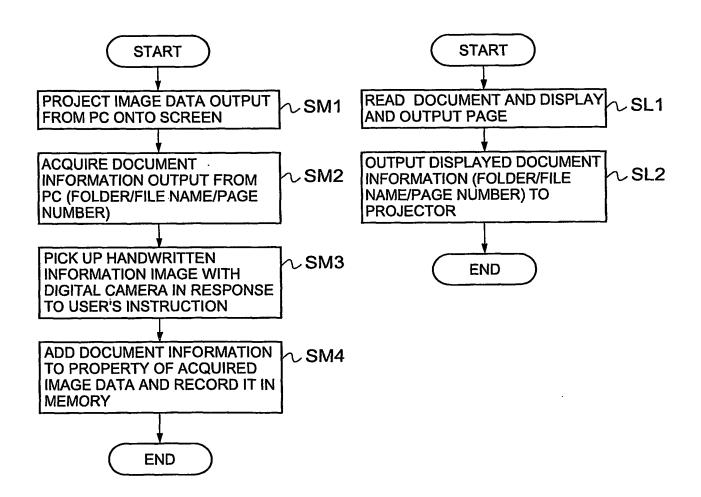


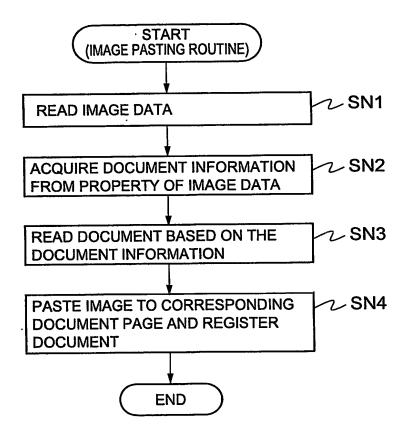
Fig. 27

300

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Fig. 28



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